WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of isolations formed on a semiconductor substrate;

a plurality of active regions defined on the semiconductor substrate and isolated from each other by the isolations;

a plurality of control gate electrodes formed over the semiconductor substrate, each said control gate electrode crossing all of the isolations and all of the active regions with a first insulating film interposed between the control gate electrode and the semiconductor substrate; and

a plurality of floating gate electrodes, each of which is formed for associated one of the active regions so as to cover a side face of associated one of the control gate electrodes with a second insulating film interposed between the floating gate electrode and the control gate electrodes,

wherein the isolations are spaced apart from each other along the width of the control gate electrodes and

wherein each said isolation crosses all of the control gate electrodes and extends continuously along the length of the control gate electrodes.

2. The device of Claim 1, further comprising a third insulating film formed on each of the control gate electrodes.

3. The device of Claim 1, wherein each of the active regions has a plurality of step regions, each of which is overlapped by associated one of the floating gate electrodes and,

wherein in each said active region, source regions are defined in respective upper parts of the step regions and a drain region is defined below the step region.

4. A method for fabricating a semiconductor memory device, comprising the steps of:

a) forming a plurality of isolations on a semiconductor substrate, thereby defining a plurality of active regions, which have been isolated from each other by the isolations, on the semiconductor substrate;

b) forming a first insulating film and a first conductive film in this order over the semiconductor substrate and then selectively etching the first conductive film, thereby forming a control gate electrode out of the first conductive film so that the control gate electrode crosses all of the isolations and all of the active regions;

c) forming a second insulating film and a second conductive film in this order over the semiconductor substrate as well as over the isolations and the control gate electrode and then selectively etching parts of the second conductive film, thereby forming floating gate electrodes out of the second conductive film for the active regions so that the

floating gate electrodes cover a side face of the control gate electrode; and

d) implanting ions into the semiconductor substrate using the control gate electrode and the floating gate electrodes as a mask, thereby defining source and drain regions in each said active region,

wherein the step c) includes:

forming and selectively etching the second conductive film to form a sidewall-shaped conductive film out of the second conductive film on the side face of the control gate electrode;

removing parts of the sidewall-shaped conductive film and parts of the second conductive film from over the isolations; and

removing remaining parts of the second conductive film from upper and another side faces of the control gate electrode, thereby forming the floating gate electrodes as islands out of the sidewall-shaped conductive film on the side of the control gate electrode.

5. The method of Claim 4, wherein the step a) comprises forming the isolations in a striped pattern on the semiconductor substrate so that the isolations are spaced apart from each other along the width of the control gate electrode.

6. The method of Claim 4, wherein the step b) comprises forming a third insulating film on the first conductive film and then etching the third insulating film and the first conductive film.

7. The method of Claim 4, wherein the step c) comprises:

forming a sidewall insulating film on side faces of the control gate electrode with the second insulating film interposed between the sidewall insulating film and the control gate electrode; and

etching parts of the semiconductor substrate, which parts are located below the side face of the control gate electrode, using the sidewall insulating film as a mask, thereby forming a plurality of step regions for the active regions.